
AFRL-RZ-WP-TP-2010-2099

# CAPACITOR CHARACTERIZATION STUDY FOR A HIGH POWER, HIGH FREQUENCY CONVERTER APPLICATION (PREPRINT)

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**APRIL 2010**



**AIR FORCE RESEARCH LABORATORY**
**PROPULSION DIRECTORATE**
**WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7251**
**AIR FORCE MATERIEL COMMAND**
**UNITED STATES AIR FORCE**

# REPORT DOCUMENTATION PAGE

*Form Approved*
*OMB No. 0704-0188*



| 1. REPORT DATE *(DD-MM-YY)* | 2. REPORT TYPE | 3. DATES COVERED *(From - To)* |
|---|---|---|
| April 2010 | Conference Paper Preprint | 04 August 2009 – 01 April 2010 |

**4. TITLE AND SUBTITLE**
CAPACITOR CHARACTERIZATION STUDY FOR A HIGH POWER, HIGH FREQUENCY CONVERTER APPLICATION (PREPRINT)

**5a. CONTRACT NUMBER**
In-house

**5b. GRANT NUMBER**

**5c. PROGRAM ELEMENT NUMBER**
62203F

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**5d. PROJECT NUMBER**
3145

**5e. TASK NUMBER**
13

**5f. WORK UNIT NUMBER**
31451314

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**

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**8. PERFORMING ORGANIZATION REPORT NUMBER**
AFRL-RZ-WP-TP-2010-2099

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
Air Force Research Laboratory
Propulsion Directorate
Wright-Patterson Air Force Base, OH 45433-7251
Air Force Materiel Command
United States Air Force

**10. SPONSORING/MONITORING AGENCY ACRONYM(S)**
AFRL/RZPE

**11. SPONSORING/MONITORING AGENCY REPORT NUMBER(S)**
AFRL-RZ-WP-TP-2010-2099

**12. DISTRIBUTION/AVAILABILITY STATEMENT**
Approved for public release; distribution unlimited.

**13. SUPPLEMENTARY NOTES**
Conference paper submitted to the Proceedings of the High Temperature Electronics (HiTEC 2010) Conference held May 11 - 13, 2010 in Albuquerque, NM. PA Case Number: 88ABW-2010-1865, 05 Apr 2010. Paper contains color. The U.S. Government is joint author of this work and has the right to use, modify, reproduce, release, perform, display, or disclose the work.

**14. ABSTRACT**
Recent advances in SiC power devices and high temperature magnetic and insulation materials has led to an increase in activity to develop compact, high switch rate power system components that can operate at temperatures in excess of 200°C. These efforts have highlighted the need to develop capacitor technology for high power, high frequency power filter applications, which can experience cycling over a wide range of temperature (-55 °C to 250 °C). A modeling and simulation capability was used to investigate device architecture and electrical performance relationships for a select group of wound and stacked devices, which were then evaluated for use in a power conditioning application. A finite element analysis of the device architectures was used to develop a better understanding of how magnetic fields and thermal profiles affect the performance of the capacitors in maintaining a low ripple voltage at high switch rates (>20 kHz). Both predicted electrical properties and empirical data were utilized as SPICE simulation input parameters to evaluate the performance of the different capacitors in an interleaved DC-DC boost converter model. Of interest is developing a better understanding of how the device architecture and its electrical properties affect its performance as a filtering device in a high power, high frequency application.

**15. SUBJECT TERMS**
high temperature, high power, capacitor, DC-DC converter, capacitor packaging

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT: | 18. NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON (Monitor) |
|---|---|---|---|---|---|
| a. REPORT | b. ABSTRACT | c. THIS PAGE | | | James Scofield |
| Unclassified | Unclassified | Unclassified | SAR | 14 | 19b. TELEPHONE NUMBER *(Include Area Code)* N/A |

**Standard Form 298 (Rev. 8-98)**
Prescribed by ANSI Std. Z39-18

# Capacitor Characterization Study for a High Power, High Frequency Converter Application

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## Abstract

*Recent advances in SiC power devices and high temperature magnetic and insulation materials has led to an increase in activity to develop compact, high switch rate power system components that can operate at temperatures in excess of 200°C. These efforts have highlighted the need to develop capacitor technology for high power, high frequency power filter applications, which can experience cycling over a wide range of temperature (-55 °C to 250 °C). A modeling and simulation capability was used to investigate device architecture and electrical performance relationships for a select group of wound and stacked devices, which were then evaluated for use in a power conditioning application. A finite element analysis of the device architectures was used to develop a better understanding of how magnetic fields and thermal profiles affect the performance of the capacitors in maintaining a low ripple voltage at high switch rates (>20 kHz). Both predicted electrical properties and empirical data were utilized as SPICE simulation input parameters to evaluate the performance of the different capacitors in an interleaved DC-DC boost converter model. Of interest is developing a better understanding of how the device architecture and its electrical properties affect its performance as a filtering device in a high power, high frequency application.*

Key words: High Temperature, High Power, Capacitor, DC-DC Converter, Capacitor Packaging

### Introduction

For many applications, electrical systems continue to evolve into higher power, more compact architectures as a means to increase performance and enhance capability. In particular, there is a concerted effort in the aviation community to develop "more electric" architectures as a means to improve the capability, reliability, and maintainability of the aircraft [1,2]. Continued progression of these developments is constrained by the size of the electrical subsystems and the requirement for thermal conditioning. An approach to ease this constraint is to develop compact, thermally robust electrical systems to reduce the thermal load to the heat pump and to enable placement of electrical technology in close proximity to heat sources (e.g., generators, motors, leading edges).

Capacitors commonly account for a large percentage of the volume and cost in the design of electrical power conditioning systems [3]. In addition, the desire to raise the upper temperature limit of capacitors has grown due to recent progress in silicon carbide technology [4], high-temperature magnetic material development [5], and the demonstration of these components in power electronics at temperatures above 200°C [6]. High-temperature polymer film capacitors tend to have desirable features such as high current carrying capability, graceful failure, and low cost. Of recent interest is manufacturing of high temperature FPE film capacitors at industrial scale [7] and the improvement in breakdown strength of acrylate-based polymer multilayer (PML) devices [8].

The availability of FPE film is expected to improve the capability to fabricate polymer film capacitors that can withstand exposure to high temperature environments and/or tolerate internal heating due to power dissipation. Alternatively,

stacked devices such as PML capacitors may be preferable for certain applications based on the equivalent series resistance (*ESR*) and equivalent series inductance (*ESL*). Such examples include high switch rate and high ripple current requirements. A thorough evaluation of these devices would require an in-depth analysis of the capacitor architecture to include packaging, material components, and their respective dimensions. These features are expected to have a notable impact on the device performance and therefore limit its potential application [9,10].

A comparison study is conducted herein between FPE, PML, and Polyphenylene Sulfide (PPS) capacitors as candidate devices for an output filter in a high switch rate interleaved boost converter. The devices used for testing include packaged and unpackaged PPS (replacement for polycarbonate capacitors [3]); packaged and unpackaged FPE capacitors; and unpackaged DPGDA (dipropylene glycol diacrylate) PML capacitors. A simplified equivalent circuit model is initially utilized to define the properties of the capacitors. Simulations are then performed using finite elemental analysis (FEA) to predict the magnetic fields and thermal profile within the devices as a means to study the parasitic inductance and heat dissipation. The modeling and simulation results are then correlated with empirical data obtained from the testing of prototype capacitors under ambient conditions. In particular, comparisons are made with respect to the impact packaging has on device characteristics such as the *ESR*, *ESL*, and resonant frequency ($\omega_{res}$). Finally, these learned characteristics are utilized with a converter simulation to evaluate the performance of the PPS, FPE, and DPGDA capacitors under high power, high frequency AC excitations.

**Capacitor Modeling for ESR and DF**

Several equivalent circuit models for a capacitor have been proposed to properly fit impedance spectroscopy data for dielectrics and capacitors [11]. For this paper, the equivalent circuit model shown in Figure 1 was assumed.

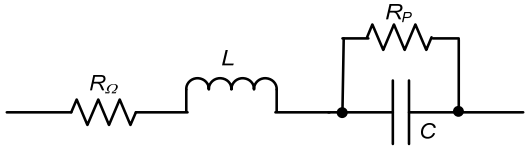


**Figure 1.** Equivalent circuit model of a capacitor.

In this model [12], $R_p$ represents the dielectric and absorption loss, $R_\Omega$ is the ohmic (series) loss, $L$ is the internal inductance, and $C$ is the capacitance.

For this study, $R_p$ represents the dielectric resistance and can be influenced by fluctuations in dipole moments, charge injection, charge carriers, electron or hole mobility, and/or thermal diffusion [11]. $R_\Omega$, the ohmic losses, are contributed by electrode resistance, solder terminations (contact) resistance, and lead resistance. $L$ is the inductance due to the induced magnetic fields within the capacitor, such as wire connections from the package terminations to the capacitor device, epoxy filled section, and the real dielectric section. It should be noted that the return current was directed around the capacitor to cancel the magnetic fields outside the device.

From this circuit model, the total circuit impedance ($Z_{cap}$) is expressed in equation (1).

$$Z_{cap}=\left(R_\Omega+\frac{R_p}{1+\omega^2C^2{R_p}^2}\right)+j\left(\omega L-\frac{\omega C{R_p}^2}{1+\omega^2C^2{R_p}^2}\right) \quad \textbf{(1)}$$

The real part of $Z_{cap}$ is *ESR*, and the imaginary part is reactance, *X*. Therefore, a dissipation factor (*DF*) can be expressed as,

$$DF=\frac{|ESR|}{|X|}=\frac{\left|R_\Omega+\frac{R_p}{1+\omega^2C^2{R_p}^2}\right|}{\left|\omega L-\frac{\omega C{R_p}^2}{1+\omega^2C^2{R_p}^2}\right|} \quad \textbf{(2)}$$

The desire is to develop an ideal model to represent the real value (*ESR*) and imaginary value (*X*) obtained from the impedance measurements wherein it is possible to derive all four values in the capacitor equivalent circuit in Figure 1. Currently, efforts to obtain all four component values inside a capacitor are underway and will be addressed in future studies.

**Table 1.** Summary of Capacitor Properties

| Characteristic \ Capacitor | FPE | PPS | DPGDA |
|---|---|---|---|
| **Dielectric** Constant | 3.0 | 3.0 @ 25°C | 4.8 |
| Thermal Cond. (W/mK) | 0.1672 | 0.129704 | ? |
| Thickness (μm) | 5 | 6 | 0.5 |
| Width (mm) | 50 | 50 | 26.43 |
| **Al Electrode** Thickness (Å) | 50 | 66.25 - 141 | ~100 |
| Al Width (mm) | 46 | 47.69 | 21.59 |
| Al Resistivity (Ω/sq) | 15 | 2 - 4 | ~2.5-3 |
| **Arc Spray Mat'l** | Zinc | Zinc & Babbitt | solder |
| Thickness (mm) | 2.54 | .9144 - 1.143 | Unknown |
| **Core Rod (mm)** | D = 1.651<br>L = 51.689 | D = 1.651<br>L = 51.689 | N/A |
| **Voltage Rating ($V_{dc}$)** | 250 | 250 | $V_{bd}$ > 200 |
| **Unpackaged Dimensions (mm)** | D = 17.8<br>L = 52.2 | D = 20.828<br>L = 50.8 | l = 26.96<br>h = 1.56<br>w = 26.43 |
| **Packaged Dimensions (mm)** | D = 25.4<br>L = 76.5 | D = 25.4<br>L = 76.5 | N/A |

**Capacitor Specifications**

In this paper, the electrical performances of wound PPS and FPE capacitors manufactured by Dearborn Electronics were evaluated in the packaged and unpackaged forms. In addition, unpackaged DPGDA multilayer capacitors by Sigma Technologies were also evaluated. Table 1 summarizes the basic properties of the capacitors. A pictorial view of a packaged and unpackaged FPE capacitor is shown in Figure 2A along with a schematic in Figure 2B. The PPS capacitors had similar device architectures, but with slightly different dimensions (not shown). A corresponding representation of the DPGDA multilayer capacitor is shown in Figure 3.

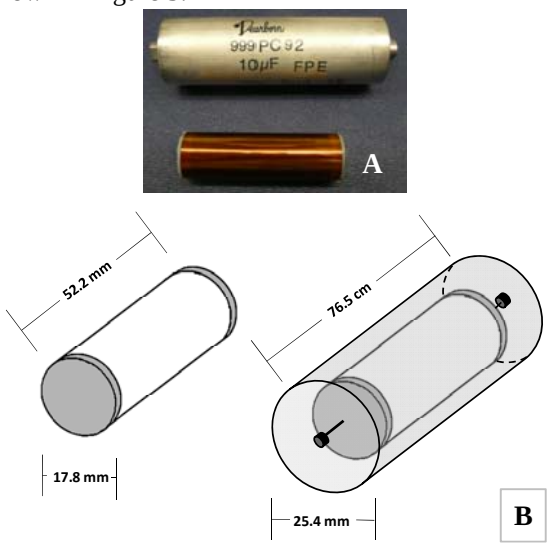


**Figure 2.** Images (A) and schematics (B) of 10 μF metallized FPE pkg'd (top) and unpkg'd (bottom) capacitors.

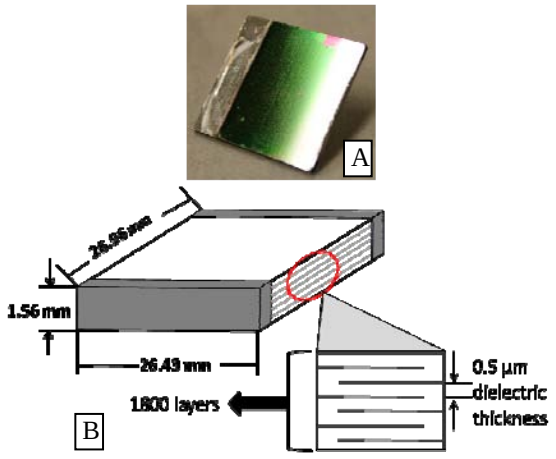


**Figure 3.** Image (A) and schematic (B) of 30 μF metallized DPGDA unpackaged capacitors studied for electrical performance evaluation.

**Modeling Simulation**

Initial finite element analysis (FEA) simulation, using *QuickField Professional* software, was utilized to predict temperature distributions and parasitic inductance for the 5 capacitor types. Since this software is *2-D* FEA, both temperature and magnetic profiles were solved for the radial cross sections at the midpoint along the capacitor length. The results of these simulations are shown in Table 2. It was assumed that 1 W of power was dissipated in the capacitors and the boundary condition for temperature of the outer surface was fixed at 300 K for all capacitor types. For these results, only thermal conduction radially through the capacitors was considered as a means of heat removal. The equivalent thermal conductivity of the FPE dielectric film was assumed to be 0.1672 W/mK and 0.548 W/mK [13] was used for the thermal conductivity of the filler epoxy in the packaged capacitors. Due to a lack of data on the thermal conductivity of DPGDA, 0.2 W/mK [14] was assumed for calculations. The data in Table 2 predicts that the peak temperature rise is 11.7 K for the unpackaged PPS capacitor, whereas the packaged PPS capacitor shows a maximum temperature rise of 12.7 K. The temperature rise for FPE and DPGDA capacitors are also found in the table. In terms of the equivalent series inductance (*ESL*), the unpackaged capacitors provide a lower predicted *ESL* than the packaged capacitors. For example, the inductance of the unpackaged PPS capacitor was 2.74 nH, whereas the predicted *ESL* of the packaged PPS geometry resulted in 10.19 nH.

**Table 2.** Summary of FEA results for the capacitor thermal and electrical performance

| Capacitor Type | PPS Unpkg'd/Pkg'd | FPE Unpkg'd/Pkg'd | DPGDA Unpkg'd |
|---|---|---|---|
| Dissipated Power (W) | 1 | 1 | 1 |
| Surface temp (K) | 300 | 300 | 300 |
| ESR (mΩ) | 5.04/12.2 | 36.3/28.8 | 30.8 |
| $L_{diel}$ (nH) | ---/4.52 | ---/6.16 | |
| $L_{ends}$ (nH) | ---/5.67 | ---/5.36 | |
| $L_{tot}$ (nH) | 2.74/10.19 | 3.15/11.52 | 1.59 |
| Max temp (K) | 311.7/312.7 | 308.8/310.7 | 301.6 |

Figures 4(A) and 4(B) show a comparison of the simulated temperature profiles for the unpackaged and packaged PPS capacitors. As expected, it is shown that the packaged capacitor architecture has a higher internal temperature rise than the unpackaged device. This higher maximum internal temperature rise for the packaged capacitor is simply due to the additional thermal resistance of the epoxy. Conversely, since the unpackaged capacitor carries no external thermal resistance due to the

epoxy part, the internal heat can be extracted more efficiently.

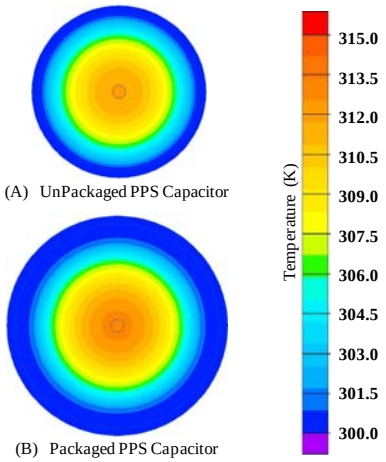


**Figure 4.** Temperature rise distribution for PPS capacitor architectures dissipating 1 W of power.

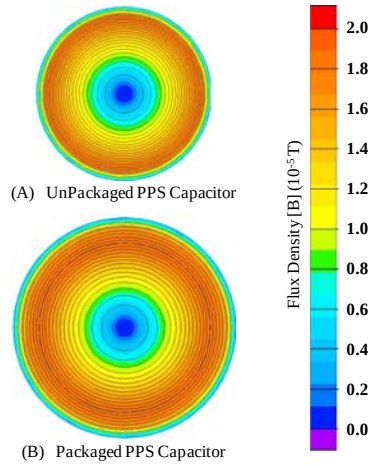


**Figure 5.** Magnetic field distribution for pkg'd and unpkg'd PPS capacitors with 1 A of current.

The cross-sectional profile of the magnetic field for the capacitors is shown in Figure 5. This simulation was performed using a simulated current of 1 A. These devices have an outer layer, which represents a copper shroud that is wrapped around each device. The copper shroud is electrically connected to the device such that the current that goes into the device follows a path out through the shroud. As a result, the magnetic field outside the capacitor is canceled. It should be noted that the magnetic fields of the wound film sections are identical between the unpackaged and packaged capacitors. Therefore, the difference in inductance for both configurations is due to the extra sections of the packaged configuration. Since the magnetic fields and the inductance of the capacitor are related by Equation 4, the lead sections and the epoxy section are responsible for the difference in inductance of the packaged capacitor as compared to the unpackaged configuration. Similar features were indicated in the cross-sectional profiles of the FPE devices, while those for the DPGDA devices did not have notable contrast in neither the temperature rise nor the magnetic field profiles.

$$\frac{1}{2}LI^2 = \frac{1}{2}\int \frac{B^2}{\mu} dv \qquad \textbf{(3)}$$

**Empirical Capacitor Measurements**

Electrical characterization was performed on three capacitors for each type indentified in the discussion above (pkg'd PPS & FPE and unpkg'd PPS, FPE, and unpkg'd DPDGA). Data was obtained from 3 devices for each type, of which the capacitor with median values was selected for representation and discussion herein. All capacitors were encased in a copper shroud during testing to minimize device inductance due to its external magnetic field.

The devices were tested under ambient conditions using an Agilent 4284A LCR meter with a 16047C test fixture. Leads connecting the capacitor to the LCR meter were 5 cm in length. Data was collected utilizing custom designed software, recording *ESR (R)* and *Reactance* (*X)* as a function of frequency, swept from 20 Hz to 1 MHz. The instrument was set with DC bias at 0 $V_{DC}$ and signal voltage at 2.7 $V_{AC}$. *DF* and *Capacitance* was calculated from the measured values of *R* and *X*.

Figure 6 shows the representative *ESR* as a function of frequency for each type of device evaluated. The metallic shroud did not appear to affect the *ESR* (not shown). Both the unpackaged and packaged PPS capacitors had the lowest *ESR* across the entire range of frequencies, which was attributed to thicker aluminum electrodes (Table 1).

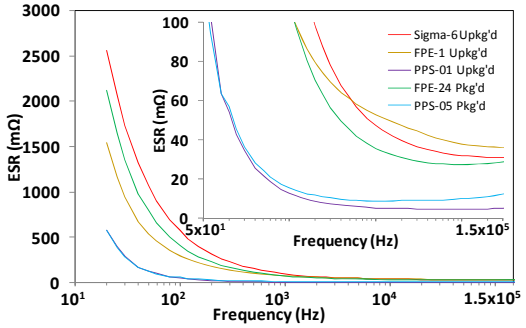


**Figure 6.** ESR as a function of frequency.

The DPGDA capacitor appeared to have the highest *ESR* value at low frequency, which decreased to a much lower value at higher frequency. The high *ESR* at low frequency may be attributed to a lower $R_p$

of the DPGDA dielectric, per the real part (*ESR*) of Equation 1. A similar effect was observed with the temperature cycling of FPE capacitors in a previous study [15]. The resistive loss mechanism may be due to displacement current (e.g., residual reactants or dipole oscillation) or conduction current at low frequency. As noted in Table 3, the DPGDA device had the lowest static (*DC*) insulation resistance among the capacitors when measured at 100 $V_{DC}$. The relatively low insulation resistance of the DPDGA device may indicate a notable impact of conduction current on $R_p$. As the frequency approached 150 kHz, the *ESR* of the DPGDA capacitor decreased to a similar value, if not lower, than that observed for the FPE devices. A lower *ESR* is expected at higher frequency due to a stronger dependence on $R_\Omega$. Since the electrode thickness was high (100 Å) and width was low (21.59 mm) for the DPGDA device in comparison to the others listed in Table 1, an even lower *ESR* could be expected. The higher than anticipated *ESR* values may be due to high contact resistance or possibly a stronger dependence upon $R_p$.

**Table 3.** Summary of DC Insulation Resistance

| Insulation Resistance (GΩ) | | |
|---|---|---|
| **Capacitor Type** | **UnPkg'd** | **Pkg'd** |
| FPE | 14.1 | 12.8 |
| PPS | 42.2 | 46.1 |
| DPGDA | 1.4 | |

At low frequency, the *ESR* of the unpackaged FPE device was lower than the value for the unpackaged version and the DPGDA capacitor. As the frequency was increased to 150 kHz, the *ESR* of the unpackaged FPE capacitor decreased to 36.3 mΩ, which was then higher than that for the packaged version (28.8 mΩ) and the DPGDA device (30.8 mΩ). The *ESR* effects of the FPE capacitors may be due to slight differences in electrode contacts or dimensions, but needs to be investigated further.

Figure 7 shows the dissipation factor (*DF*) for each device as a function of frequency. The *DF* is defined in Equation 4 as a ratio of the resistive loss (*ESR*) in the device versus the energy stored by the reactive components. As observed in Figure 7, the *DF* of the PPS devices remained less than 0.1% at low frequency (20 Hz to 2 kHz), which correlates with its low *ESR*. Similarly, the higher *DF* for the FPE devices corresponded to its *ESR* values at low frequency. The *DF* for DPGDA was the highest across the range of frequencies as it increased from 1% at 20 Hz up to 100% at 150 kHz. At higher frequencies, the *DF* increases to very high values since the magnitude of the reactive component approaches zero, which eventually approaches the resonant frequency ($\omega L = 1/\omega C$). Therefore, the *DF* for the packaged devices (i.e., FPE and PPS) is observed to increase at a more rapid rate due to a larger inductance.

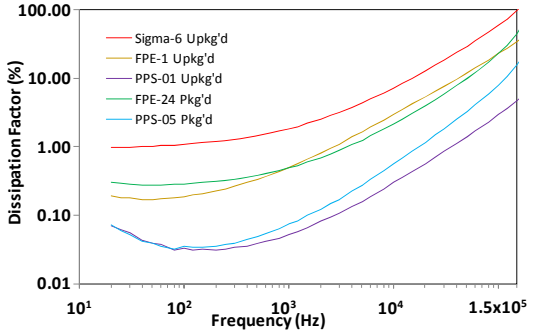


**Figure 7.** DF as a function of frequency.

Figure 8 shows the effective capacitance values ($C=1/\omega X$) as a function of frequency. As shown, PPS and FPE remained constant up to 50 kHz. For DPGDA, there was a 4.3% decrease in the effective capacitance going from 20 Hz to 50 kHz. For all capacitors in Figure 8, the rapid increase in effective capacitance at frequencies greater than 50 kHz is an artifact as the capacitor approaches its resonant frequency. Similarly, low values of $R_p$ cannot be neglected, since it may cause an increase in the series capacitance. As seen in Equation 5, as $R_p$ approaches zero, $C_s$ increases. The $R_p$ effect can be demonstrated by measuring a capacitor in parallel with a low ohm resistor, thus resulting in a higher capacitance reading.

$$C_s = \frac{1+\omega^2 C^2 {R_p}^2}{\omega^2 C {R_p}^2} \quad \textbf{(4)}$$

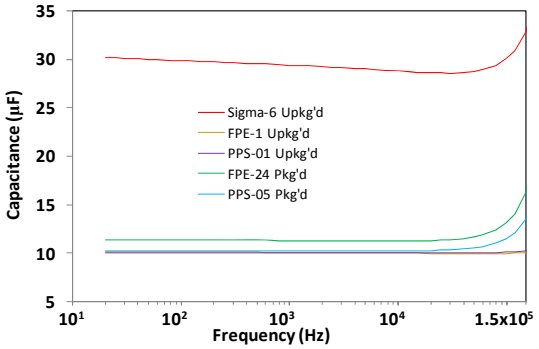


**Figure 8.** Effective Capacitance as a function of frequency.

As stated above, the point where reactance changes from a negative to a positive value is considered the resonant frequency of the device. Thus, by taking the imaginary (*reactance-X*) term in

Equation 1 above and equating this term to 0 will yield the resonant frequency as shown in Equation 6.

$$\omega_{res} = \sqrt{\frac{1}{(L_S * C)} - \frac{1}{C^2 * R_p{}^2}} \qquad \textbf{(5)}$$

Table 4 shows the measured resonant frequencies for the unpackaged and packaged capacitors, with and without a copper shroud. The added shroud effectively decreases the inductance by cancelling external magnetic fields, thus increasing the resonant frequency and capacitor operating range. The shroud had minimal impact on the values of *ESR* and capacitance.

**Table 4.** Summary of the Resonant Frequency

| | $f_{res}$ (kHz) | w/o shroud | w/Cu shroud |
|---|---|---|---|
| UnPkg'd | **FPE-1** | 140.714 | >1 MHz |
| | **PPS-01** | 154.321 | 933.964 |
| | **SIGMA-6** | 459.814 | 401.131 |
| Pkg'd | **FPE-24** | 183.144 | 274.731 |
| | **PPS-05** | 197.073 | 315.168 |

Table 5 lists the calculated inductance values for the capacitors based on the measured resonant frequency. For this calculation, the second term of Equation 6 was assumed to be negligible due to a large $R_p$. The capacitance value at 20 Hz was chosen and is assumed to be a constant for these calculations. For comparison purposes, the resonant frequency, as determined from the simulation, is also listed.

**Table 5.** Calculated vs Simulated Inductance Values

| $L_s$-$C_s$ Table | | Measured | Calculated Data | | | |
|---|---|---|---|---|---|---|
| | | 20 Hz | **Resonant Freq.** | | **Simulated Data** | |
| | | $C_s$ (µF) | $f_{res}$ (kHz) | $L_s$ (nH) | $Ls$ (nH) | $f_{res}$ (kHz) |
| UnPkg'd | **Sigma-6** | 30.2 | 401.13 | 5.21 | 1.59 | 726.30 |
| | **FPE-1** | 10.1 | *1100.00* | 2.07 | 3.15 | 892.29 |
| | **PPS-01** | 10.0 | 933.96 | 2.90 | 2.74 | 961.49 |
| Pkg'd | **FPE-24** | 11.4 | 274.73 | 29.44 | 11.52 | 439.18 |
| | **PPS-05** | 10.2 | 315.17 | 25.00 | 10.19 | 493.67 |

**DC/DC Converter Simulation**

The *ESR* and *L* effect of a filtering capacitor on the output ripple voltage of a DC-DC converter is considered next. Power dissipation in capacitors due to the AC current through it and the associated temperature rise are also discussed.

Figure 9 shows an inverse-coupled two-phase interleaved DC-DC boost converter suitable for high performance, high power applications [16]. A 100 V/270 V, 10 kW boost converter with a duty ratio of 0.67 and a switch frequency of approximately 75 kHz is considered for evaluating the effects of an output filter capacitor's ($C_{out}$) *ESR* and *ESL* on the converter output ripple voltage, capacitor power loss, and temperature rise.

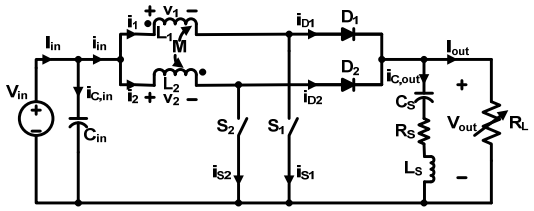


**Figure 9.** Circuit schematic of an inverse-coupled two-phase interleaved DC-DC converter.

For evaluating FPE, PPS, and DPGDA capacitor performance, several combinations of capacitors resulting in total capacitance of 40 µF are considered and compared. In this simulation, the capacitor was assumed to have $R_s$, $L_s$, and $C_s$ as shown in Figure 9. $L_s$ in this section is identical to $L$ in Equation 1, $R_s$ is the real part of Equation 1 and $C_s$ is related to $C$ by Equation 5.

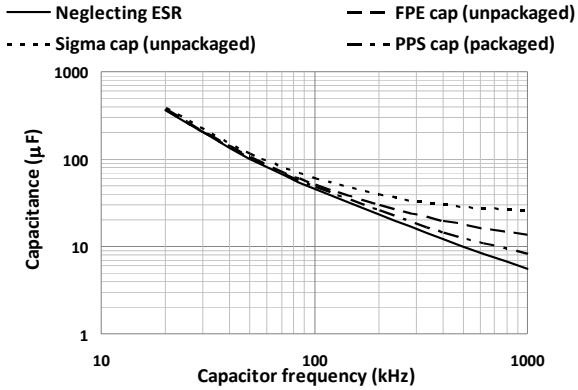


**Figure 10.** Required total output capacitance as a function of frequency when $V_{pp}$ = 2.7 V.

Since the interleaved converter described above works as a dual phase converter, the actual capacitor frequency is twice the operating frequency (150 kHz). Using SPICE simulation, the required total output filter capacitance to maintain a ripple voltage of 2.7 V as a function of frequency is shown in Figure 10 above. For this comparison, it was assumed that only one FPE or PPS capacitor are required to hold the output voltage of 270 V, but three DPGDA capacitors in series are required for the same output voltage. In Figure 10, it is shown that larger capacitances are required to reduce the increase in the ripple voltage caused by the larger *ESR*. Although it is not shown in the figure, including inductance for these capacitors did not change the required capacitance values.

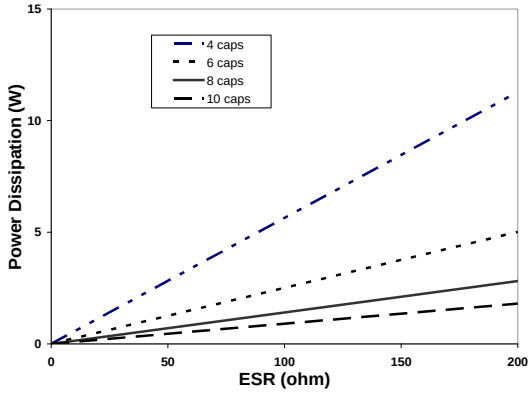


**Figure 11.** Power dissipation in an individual capacitor as a function of its *ESR* for various numbers of capacitor in parallel.

Figure 11 shows the power dissipated in each capacitor as a function of *ESR* when a group of capacitors in parallel are used as the output capacitor for the DC-DC converter. Using *ESR* values in Table 2, the internal temperature rise of the capacitor can be predicted. For the PPS packaged capacitor with *ESR* of 12.2 mΩ the dissipated power and maximum internal temperature rise are 0.69 W and 8.74 K, if 4 capacitors are used in parallel. Further, the dissipated power and temperature rise for each capacitor in a group of six, eight and ten capacitors are 0.31 W (3.9 K), 0.17 W (2.2 K) and 0.11 W (1.4 K), respectively. For the packaged FPE capacitor with 22.8 mΩ *ESR*, the corresponding values for each capacitor for 4, 6, 8 and 10 capacitors in parallel are 1.62 W (17.4 K), 0.72 W (7.7 K), 0.41 W (4.3 K), and 0.26 W (2.8 K), respectively. Due to the voltage rating of the DPGDA capacitor, three DPGDA capacitors connected in series were considered. For 12 DPGDA capacitors (4 parallel sets of DPGDA capacitors connected 3 in series) the power dissipation and corresponding temperature for each capacitor is 1.74W (2.78K). If 18, 24 and 30 DPGDA capacitors are used, the corresponding values are 0.77W (1.23K), 0.43W (0.69K), and 0.27W (0.44K), respectively. It should be mentioned that the power dissipation in each capacitor is proportional to the square value of the current; therefore by multiplying the number of capacitors by a factor of two, the dissipation power on each capacitor will be reduced by a factor of four.

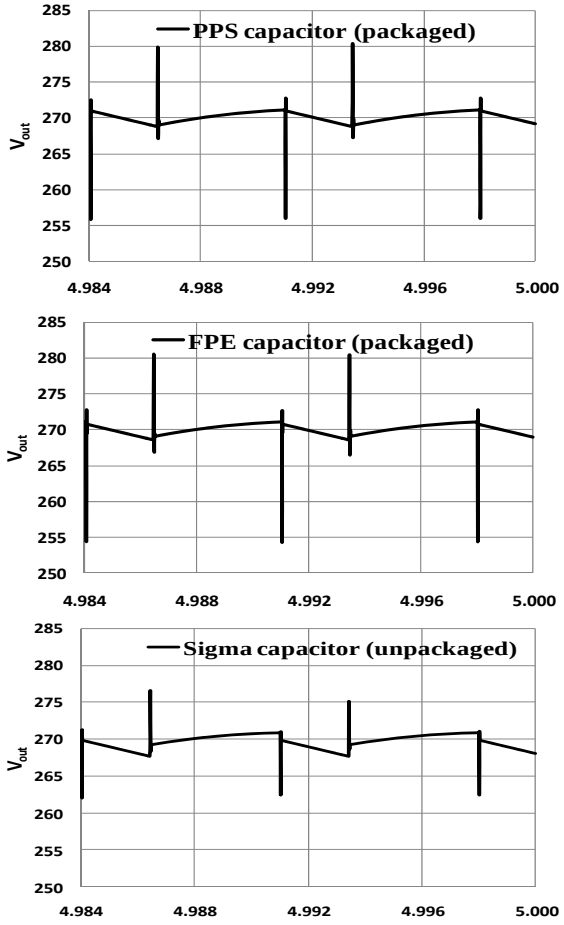


**Figure 12.** Output Voltages of FPE, and PPS packaged capacitors and Sigma capacitor for a 100 V/270 V, 10 kW, 75 kHz interleaved DC-DC converter. 4 -10 uF capacitors were connected in parallel for FPE and PPS Figures. For Sigma capacitors, a total of 12 capacitors are used. (3 in series and 4 in parallel).

Figure 12 shows the output voltages for FPE, PPS packaged capacitors and the DPGDA capacitor. These Figures show the effects of inductance and *ESR*. The difference in both the voltage spikes and ripples for FPE and PPS packaged capacitors is not significant. The harsh spikes take place when the direction of current into the capacitor changes. At that time, *L*di/dt* becomes very large. The magnitude for the FPE and PPS packaged capacitors are nearly identical due to similar inductance values. Although the *ESR* values for FPE and PPS are different, *I*ESR* is not large enough to make a clear difference. However, the DPGDA capacitor clearly shows greater bulk ripples and less spikes compared to the FPE and PPS packaged capacitors. These are due to greater *ESR* and smaller *ESL* of the DPGDA capacitor. It should be

mentioned here that reducing the internal inductance of the capacitor is very important for not only increasing the operating frequency of the capacitor but reducing the unnecessary noise.

**Conclusions**

FPE, PPS, DPGDA capacitors were simulated, tested, and evaluated for satisfying design constraints of a high-frequency, high-power, compact DC-DC converter. Using modeling and simulation, an accurate estimate of a capacitor's equivalent series inductance and temperature rise were achieved. Both packaged and unpackaged PPS and FPE capacitors along with unpackaged DPGDA capacitors were experimentally studied with simulation results indicating that reducing *ESR* and *ESL* is necessary in terms of minimizing output noise and temperature rise. Use of a return current shroud demonstrated that the resonant frequency of a capacitor can be increased substantially by lowering the total inductance, thus increasing the useful operating frequency for the capacitor with a corresponding reduction in the dissipation factor, or power loss and temperature rise at higher frequencies. This demonstrates the importance that must be placed on capacitor packaging and termination for higher frequency operation. A methodology to evaluate the electrical and thermal performance of a capacitor in a *DC-DC* converter application using both finite element analysis and SPICE simulation packages is established. The importance of a low *ESR* and *ESL* capacitor design is highlighted for high temperature, high power, high performance *DC-DC* power converter applications. Using the tools presented in this paper, it is possible to predict how a capacitor will perform thermally and electrically within a power converter system.

**Acknowledgements**

We would like to thank Dearborn Electronics and Sigma Technologies for supplying the capacitors and providing necessary device information.

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